Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A magnetically differential input circuit to couple a single-ended signal source to a single-ended receiving circuit, the input circuit comprising:

a first terminal to couple to an output of the single-ended signal source;

a second terminal to couple to a signal return;

a third terminal to couple to [[an]] the output of the single-ended signal source;

a first loop comprising the first terminal and the second terminal; and

a second loop comprising the second terminal and the third terminal.

Claim 2 (original): The magnetically differential input circuit defined in Claim 1, wherein the first loop and the second loop circumscribe substantially equal areas and are arranged so that a first interfering signal induced in the first loop by a source of interference is cancelled by a second interfering signal induced in the second loop by the source of interference.

Claim 3 (previously presented): A magnetically differential input circuit as defined in Claim 2, further comprising:

an input node to couple to the receiving circuit;

a common node;

a first conductor coupling the first terminal to the input node;

a second conductor coupling the third terminal to the input node; and

a third conductor coupling the third terminal to the first terminal.

Claim 4 (original): A magnetically differential input circuit as defined in Claim 3, wherein:

the first loop comprises:

the first terminal;

the input node;

the first conductor;

the second terminal; and

a first segment of the third conductor; and wherein:

the second loop comprises:

the second terminal;

the input node;

the second conductor;

the third terminal; and

a second segment of the third conductor.

Claim 5 (original): A magnetically differential input circuit as defined in Claim 3, further comprising:

a terminating impedance coupled between the input node and the second terminal.

Claim 6 (original): A magnetically differential input circuit as defined in Claim 5, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the terminating impedance;

the second terminal; and

a first segment of the third conductor; and wherein:

the second loop comprises:

the second terminal;

the terminating impedance;

the input node;

the second conductor;

the second terminal; and

a second segment of the third conductor.

Claim 7 (previously presented): A magnetically differential input circuit as defined in Claim 1, wherein the first, second and third terminals are substantially collinearly juxtaposed and the second terminal is disposed intermediate between, and substantially equidistant from, the first terminal and the third terminal.

Claim 8 (original): The magnetically differential input circuit defined in Claim 7, wherein the first loop and the second loop circumscribe substantially equal areas and are arranged so that a first interfering signal induced in the first loop by a source of interference is cancelled by a second interfering signal induced in the second loop by the source of interference.

Claim 9 (original): A magnetically differential input circuit as defined in Claim 8, further comprising:

a terminating impedance coupled between an input node and the second terminal.

Claim 10 (original): A magnetically differential input circuit to couple a source of differential signals to a differential receiving circuit, the input circuit comprising:

a first terminal to couple to a first output of the source of differential signals;

a second terminal to couple to a second output of the source of differential signals;

a third terminal to couple to the first output of the source of differential signals;

an input node;

a return node;

a first conductor coupled to the first terminal and the input node;

a second conductor coupled to the first terminal and the input node, wherein the terminals, circuit nodes and conductors are arranged to form a first loop and a second loop that effect cancellation of an induced interfering voltage at the receiving circuit.

Claim 11 (original): A magnetically differential input circuit as defined in Claim 10, the first loop circumscribes a first area that is substantially equal to a second area circumscribed by the second loop.

Claim 12 (previously presented): A magnetically differential input circuit as defined in Claim 11, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of a third conductor.

Claim 13 (previously presented): A magnetically differential input circuit as defined in Claim 12, wherein the second loop comprises:

the second terminal;

the return node;

the input node;

the second conductor;

the third terminal; and

a second segment of the third conductor.

Claim 14 (original): A magnetically differential input circuit as defined in Claim 13, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of the third conductor.

Claim 15 (previously presented): A magnetically differential input circuit as defined in Claim 10, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of a third conductor.

Claim 16 (original): A magnetically differential input circuit as defined in Claim 15, wherein the second loop comprises:

the second terminal;

the return node;

the input node;

the second conductor;

the third terminal; and

a second segment of the third conductor.

Claim 17 (original): A magnetically differential input circuit as defined in Claim 16, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of the third conductor.

Claim 18 (original): A magnetically differential input circuit as defined in Claim 11, further comprising:

a first terminating resistance coupled between the input node and the return node; and

a second terminating resistance coupled between the return node and the second terminal.

Claim 19 (previously presented): A magnetically differential input circuit as defined in Claim 18, where:

the first loop comprises the first terminating resistance and the second terminating resistance; and

second loop comprises the first terminating resistance and the second terminating resistance.

Claim 20 (previously presented): A magnetically differential input circuit as defined in Claim 19, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of a third conductor.

Claim 21 (original): A magnetically differential input circuit as defined in Claim 19, wherein the second loop comprises:

the second terminal;

the return node;

the input node;

the second conductor;

the third terminal; and

a second segment of the third conductor.

Claim 22 (original): A magnetically differential input circuit as defined in Claim 21, wherein the first loop comprises:

the first terminal;

the first conductor;

the input node;

the return node;

the second terminal; and

a first segment of the third conductor.

Claim 23 (previously presented): A magnetically and electrically differential input circuit to couple to a differential signal source, the input circuit comprising:

a first input node to couple to a first polarity signal from the signal source;

a second input node to couple to a second polarity signal from the signal source;

a first terminal coupled to the first input node;

a second terminal coupled to the second input node;

a third terminal coupled to the first input node; and

a fourth terminal coupled to the second input node, wherein the first terminal and the fourth terminal are included in a first loop and wherein the second terminal and the third terminal are included in a second loop that opposes the first loop.

Claim 24 (original): An input circuit as defined in Claim 23, further comprising:

coupling means in proximity to the first, second, third and fourth terminals for balancing coupling to the first, second, third and fourth terminals.

Claim 25 (original): An input circuit as defined in Claim 24, wherein the coupling means comprises a fifth terminal and a conductor disposed between the second terminal and the fourth terminal.

Claim 26 (original): An input circuit as defined in Claim 25, wherein the fifth terminal is coupled to GND.

Claim 27 (original): An input circuit as defined in Claim 25, wherein the coupling means comprises a sixth terminal and a conductor disposed in proximity to the first terminal.

Claim 28 (original): An input circuit as defined in Claim 27, wherein the sixth terminal is coupled to GND.

Claim 29 (original): An input circuit as defined in Claim 28, wherein the coupling means comprises a seventh terminal and a conductor disposed in proximity to the third terminal.

Claim 30 (original): An input circuit as defined in Claim 29, wherein the seventh terminal is coupled to GND.

Claim 31 (original): An input circuit as defined in Claim 24, further comprising:

first terminating impedance coupled between the first terminal and the fourth terminal; and

second terminating impedance coupled between the second terminal and the third terminal.

Claim 32 (original): An input circuit as defined in Claim 31, further comprising a conductor coupled between the first terminal and the third terminal.

Claim 33 (original): An input circuit as defined in Claim 32, wherein the first terminating impedance comprises:

a first resistance coupled between the first terminal and GND; and

a second resistance coupled between GND and the fourth terminal.

Claim 34 (previously presented): An input circuit as defined in Claim 33, wherein the second terminating impedance comprises:

a third resistance coupled between the second terminal and GND; and

a fourth resistance coupled between GND and the third terminal.

Claims 35-48 (canceled)

Claim 49 (new): An input circuit comprising:

a first loop including a first terminal to receive a signal from a signal source and a second terminal to couple to a signal ground; and

a second loop including a third terminal to receive the signal from the signal source and the second terminal, wherein the first and second loops are arranged so that a first interfering signal induced in the first loop by an interference source is cancelled by a second interfering signal induced in the second loop by an interference source.

Claim 50 (new): The input circuit of claim 49, wherein the first loop physically matches the second loop.

Claim 51 (new): The input circuit of claim 50, wherein the first and second loops circumscribe substantially equal areas.

Claim 52 (new): The input circuit of claim 49, wherein the first, second and third terminals are substantially collinear and the second terminal is disposed intermediate between, and substantially equidistant from, the first terminal and the third terminal.

Claim 53 (new): The input circuit of claim 49, wherein the first and second loops effect cancellation of an induced interfering voltage at a receiving circuit coupled to the input circuit.

Claim 54 (new): The input circuit of claim 49, wherein the first, second and third terminals comprise pins on an integrated circuit package, the integrated circuit package including a transceiver.

Claim 55 (new): The input circuit of claim 54, wherein the first and third terminals are diametrically opposite and mutually adjacent to the second terminal.

Claim 56 (new): The input circuit of claim 54, wherein the first and second loops traverse an input of the transceiver in opposite directions.

Claim 57 (new): The input circuit of claim 54, further comprising a third loop within the integrated circuit package, wherein the first interfering signal induced in the first loop

by the third loop is to cancel the second interfering signal induced in the second loop by the third loop.